Design House for Digital Signal Processing

Relcom IQ Demodulator IP Core

Product description

1. IQ Demodulator

Relcom's IQ Demodulator IP Core is a high speed quadrature modulation receiver component. The core accepts analog samples of the baseband I and Q channels of a quadrature modulated signal. The input samples can be provided by an external high speed analog to digital converter (ADC) sampling the output of an analog quadrature down converter module, or by the digital samples of a digital down converter unit. The output of the core are the I and Q samples of the correctly timed and de-rotated coordinates of the symbols (soft decision) or the modulation scheme dependent raw bit combination (hard decision). The samples are provided through a received symbol rate synchronous 2x8 bit IQ bus, or through a FIFO synchronized microprocessor interface. Can be suited for decomposition of input bandpass signal into its complex envelope.

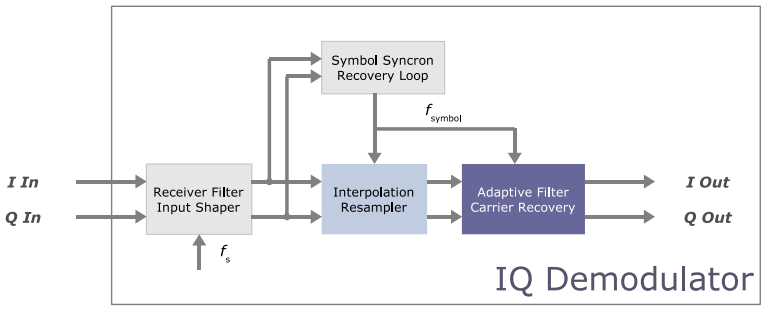

Figure 1: *General functional diagram of demodulator*

1.1. Overall Features

- Modulation schemes supported: BPSK, QPSK, OQPSK, 8PSK, 16QAM
- Symbol rate: 2k-4M symbol/sec, using 64MHz clock and sampling frequency
- Receive filter: 65 or 129 tap FIR filter operating at 8x symbol rate sample frequency, utilizing 4 times bandwidth suppression range
- Switchable DC remove component
- Forward coupled, switchable automatic gain control
- Interpolating resampling method calculating mid sample values, to get the value of the ideal sampling time
- Symbol timing recovery utilizing 24 bit filter phase locked loop, with configurable loop gain
- Adaptive filter: 8 tap complex data coefficient FIR filter operating at 2x symbol rate, synchronous to the received symbol timing
- Digital COSTAS loop utilizing CORDIC algorithm for angle measurement, with switchable loop filter coefficients
- External COSTAS loop support
- Programmable lock detector through the microprocessor interface
- Highly configurable measurement support through DA channels, with switchable measurement point on critical signals

- The whole operation is controlled through registers on the microprocessor interface
- The core fits in Xilinx Spartan3-1500 FPGA, that can be found on the PCDSP6 card, and can utilize the high speed AD units on the board. The microprocessor interface connects to the EMIF-B bus of the Texas DSP processors on the card.

2. Contact

If you have any question related to our products please do not hesitate to contact us

Relcom, Ltd.
Address: H-1112, Budapest, Táska u. 17., Hungary
Phone: +36 30 201 9919
Fax: +36 1 246 1240
Mail: info@relcom.hu
Web: http://www.relcom.hu