Design House for Digital Signal Processing

Relcom Digital Down Converter IP Core

Product description

1. Digital Down Converter

The Digital Down Converter IP Core can be suited for decomposition of input bandpass signal into its complex envelope.

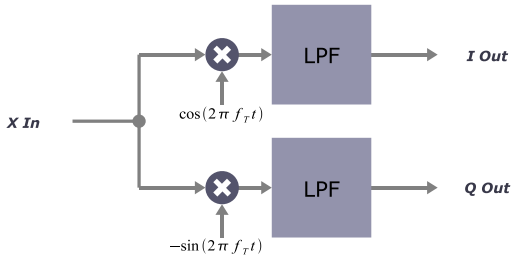

Figure 1: *General functional diagram of the down converter*

1.1. Overall Features

- 14-bit input and output word length
- 32-bit frequency resolution DDS-based transponder
- One third order CIC decimator and third order CIC interpolator for each channel
- Wide range real-time variable filter characteristics
- Automatic gain corrector for each channel
- Input and output sample rate are equal to the clock
- Direct access to the configuration parameters through individual ports
- Possible Applications
- Communication systems
- Sofware defined radios
- Channel access in all-digital receivers
- Quadrature demodulators
- Direct signal processing of carrier-based signals
- Signal processing with an orthogonal decomposition of bandpass input signals, in the baseband
- Replacement of analog DDC front-end with the advantages of stability, equal gain and linearity for I,Q channels, at a lower cost

The DDC IP core implements the general model shown in Figure 1, via the structure in Figure 2.

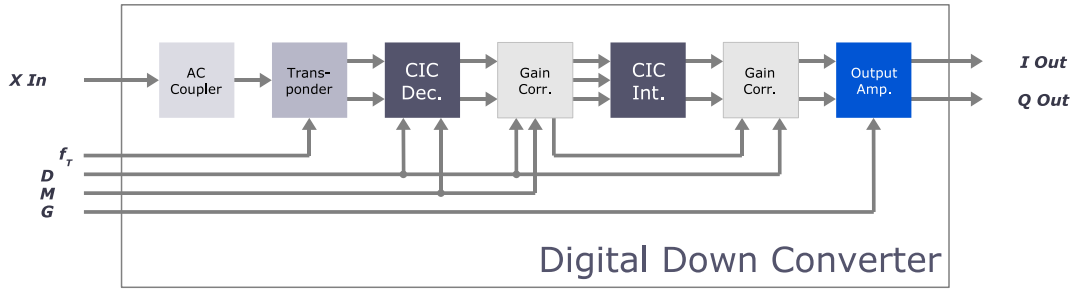

Figure 2: *Block diagram of the DDC IP core*

The core datapath comprising an AC coupler, followed by a DDS-based transponder, a series cascade of a decimator CIC filter and an interpolator CIC filter, two gain corrector units, and an output amplifier, for each channel: AC coupler pass the input frequency range above $20Hz$.

The transponder is a one-tap FIR fed back, two-phase DDS oscillator with the mixer units. The transponder frequency (fT) can be tuned real-time.

Third order decimator CIC filters have a variable decimation rate from 1 to 4092 (D), and a variable delay of the differentiators' feedthrough from 1 to 16 (M), real-time each. Third order interpolator CIC filters interpolate the decimated signal up to the input sample rate. The filter structure is shown in Figure 3. Overall filter gain remains in the range of $G * [0.5, 1]$ for every filter settings. Output amplifier have a selectable gain $G = 1, 2, 4, 8$.

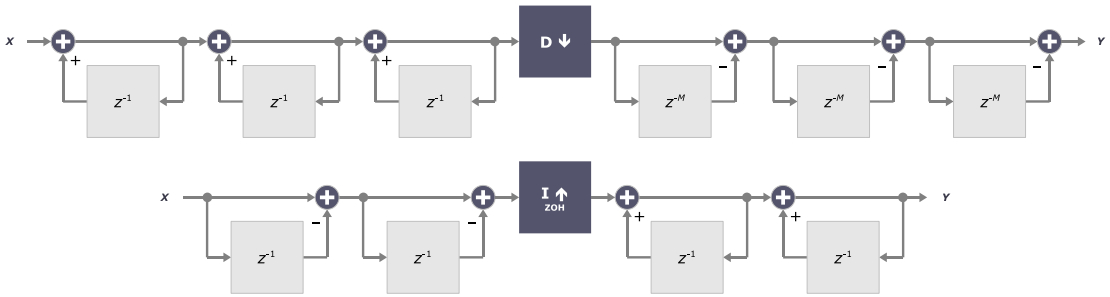

Figure 3: *Decimator and interpolator CIC filter*

The overall filter characteristic for the baseband pre-envelope components (neglect the overlap caused by the decimation) is:

$$H_{(\vartheta)} = G_c R_D^{N_D} R_I^{N_I - 1} \left(\frac{\frac{\vartheta}{2} \sin\left(\frac{\vartheta R_D}{2}\right)}{\frac{\vartheta R_D}{2} \sin\left(\frac{\vartheta}{2}\right)} \right)^{N_D} \left(\frac{\frac{\vartheta}{2} \sin\left(\frac{\vartheta R_I}{2}\right)}{\frac{\vartheta R_I}{2} \sin\left(\frac{\vartheta}{2}\right)} \right)^{N_I} e^{-j\vartheta\left(\frac{R_D + R_I}{2} + 1\right)} e^{-j17\vartheta} \quad (1)$$

$$R_D = DM, R_I = D, N_D = 3, N_I = 3, \vartheta = 2\pi \frac{f}{f_s} \quad (2)$$

where the gain correction constant $c = \frac{1}{2^{\lceil \log_2 R_D^{N_D} R_I^{N_I - 1} \rceil}}$ is provided by the gain corrector unit.

1.2. Resources

- ~ 1759 Slice in Xilinx Spartan-3 (*), ~ 1761 Slice in Xilinx Virtex-II
- 2 embedded multipliers
- 2 18 kbit BlockRAMs

2. Contact

If you have any question related to our products please do not hesitate to contact us

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